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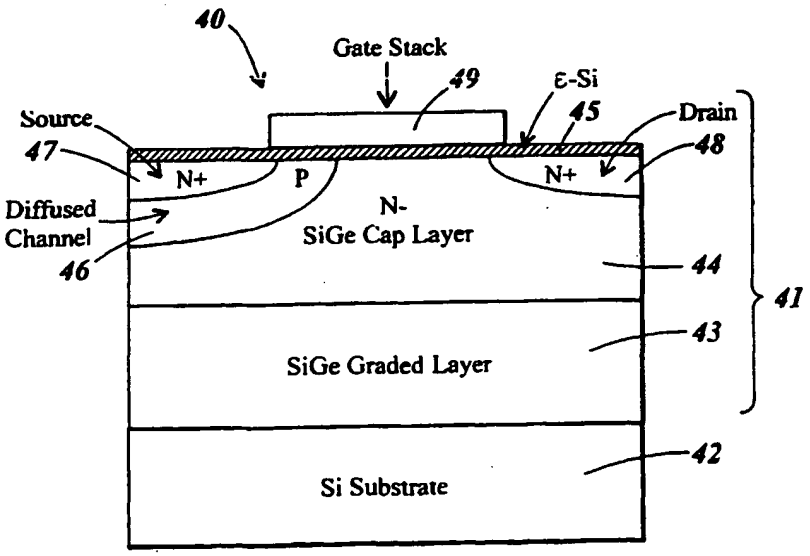
(54) Title: STRAINED-SILICON METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS



(57) Abstract: A DMOS field effect transistor fabricated from a SiGe heterostructure and a method of fabricating same. The heterostructure includes a strained Si layer on a relaxed, low dislocation density SiGe template. In an exemplary embodiment, the DMOS FET includes a SiGe/Si heterostructure on top of a bulk Si substrate. The heterostructure includes a SiGe graded layer, a SiGe cap of uniform composition layer, and a strained Si channel layer. In accordance with another embodiment, the invention provides a heterostructure for a DMOS transistor, and method of fabricating same, including a monocrystalline Si substrate, a relaxed uniform composition SiGe layer on the substrate; a first strained-Si channel layer on the uniform composition SiGe layer, a SiGe cap layer on the strained-Si channel layer, and a second strained-Si layer on the cap layer.

WO 01/54202 A1

Figure 1 is commonly referred to as a lateral DMOS (LDMOS) transistor. A device with its terminals on the front and backside of the wafer is referred to as a vertical DMOS (VDMOS) transistor. The descriptions and embodiments of the invention are best described in the LDMOS configuration. Even within the LDMOS category, there are further variations on the LDMOS transistor that incorporate different doping concentrations in the channel region. With reference to Figures 2A-2C, there are shown schematics of different doping profiles in an LDMOS transistor channel. Figures 2A and 2B show asymmetric doping profiles, and Figure 2C shows a symmetric doping profile.

Although Si-based devices, including Si DMOS, have supplanted III-V compound devices in many microelectronics markets, the inherent speed limitations of Si still prevent it from displacing III-V compound devices in a number of very high-speed applications. To address the limitations of Si, novel device heterostructures can be implemented with SiGe alloys to allow Si to extend its roadmap and continue to provide better performance in an economical manner, an essential combination for future communications systems.

Figure 3 is a schematic of the wireless communications spectrum with a snapshot of current materials technologies and anticipated materials technologies. SiGe-based electronics are predicted to play a heavy role in future wireless communications electronics.

SUMMARY OF THE INVENTION

The invention provides a DMOS field effect transistor fabricated from a SiGe heterostructure and a method of fabricating same. The heterostructure includes a strained Si layer on a relaxed, low dislocation density SiGe template. In an exemplary embodiment, the DMOS FET includes a SiGe/Si heterostructure on top of a bulk Si substrate. The heterostructure includes a SiGe graded layer, a SiGe cap of uniform composition layer, and a strained Si channel layer.

In accordance with one embodiment, the invention provides a heterostructure for a DMOS transistor, and method of fabricating same, including a monocrystalline Si substrate, a relaxed SiGe uniform composition layer on the substrate, and a strained-Si channel layer on the uniform composition layer. The heterostructure can be implemented into an integrated circuit.

In accordance with another embodiment, the invention provides a heterostructure for a (DMOS) transistor, and method of fabricating same, including a monocrystalline Si substrate, a relaxed SiGe uniform composition layer on the substrate, a first strained-Si channel layer on the uniform composition layer, a SiGe cap layer on the strained-Si channel

FET 40 in accordance with the invention. The FET includes a SiGe/Si heterostructure 41 on top of a bulk Si substrate 42. The heterostructure includes a SiGe graded layer 43, a SiGe cap of uniform composition layer 44, and a strained Si (ε-Si) channel layer 45. The device also includes a diffused channel 46, a source 47, a drain 48, and a gate stack 49.

The layers are grown epitaxially with a technique such as low-pressure chemical vapor deposition (LPCVD). The SiGe graded layer 43 employs technology developed to engineer the lattice constant of Si. See, for example, E.A. Fitzgerald *et. al.*, J. Vac. Sci. Tech. B **10**, 1807 (1992), incorporated herein by reference. The SiGe cap layer 44 provides a virtual substrate that is removed from the defects in the graded layer and thus allows reliable device layer operation. The strained Si layer 45 on top of the SiGe cap is under tension because the equilibrium lattice constant of Si is less than that of SiGe. It will be appreciated that the thickness of the Si layer is limited due to critical thickness constraints.

The tensile strain breaks the degeneracy of the Si conduction band so that only two valleys are occupied instead of six. This conduction band split results in a very high in-plane mobility in the strained Si layer (~2900cm^2/V-sec with 10^{11}-$10^{12}cm^{-2}$ electron densities, closer to 1000 cm^2/V-sec with $>10^{12}cm^{-2}$ electron densities). By using the high mobility, strained silicon for the channel region of a DMOS device, the device speed can be improved by 20-80% at constant gate length. Unlike GaAs high mobility technologies, strained silicon DMOS devices can be fabricated with standard silicon DMOS processing methods and tools. This compatibility allows for significant performance enhancement at low cost.

Semiconductor heterostructures have been utilized in various semiconductor devices and materials systems (AlGaAs/GaAs for semiconductor lasers and InGaAs/GaAs heterojunction field effect transistors). However, most of the semiconductor devices and materials systems based on heterostructures utilized schemes that allowed the entire structure to be nearly lattice-matched, i.e., no defects are introduced due to the limited strain in the epitaxial layers. Defect engineering in the late 1980s and early 1990s enabled the production of non-lattice-matched heterostructures. Of particular importance in the field of lattice-mismatched epitaxy is the relaxed SiGe on Si substrate heterosystem, which has numerous possibilities for novel device operation from high-speed transistors to integrated optoelectronics.

If the SiGe is relaxed, i.e., strain free, and the Si is strained, then the band alignment allows confinement in the conduction band, as shown in Figure 5. Figure 5 is a schematic depiction of the band offset for strained Si on relaxed SiGe. When brought to practice, the bandgap misalignment allows for electron confinement in the strained Si layer. The strained

A DMOS transistor can be modeled as an enhancement mode device in series with a depletion mode device. Figure 8 is a schematic circuit diagram of an enhancement/depletion mode model DMOS transistor 80 in accordance with an exemplary embodiment of the invention. Since devices for analog application are typically operated in the saturation regime, three possible modes of operation can be anticipated: the enhancement mode channel in saturation, the depletion mode channel in saturation, and both the depletion mode and enhancement mode channels in saturation. For best performance, the depletion mode must be in saturation; therefore, the two favorable operating regimes are depletion mode channel saturated, and depletion mode and enhancement mode channels saturated concurrently.

For the case where the depletion mode channel is saturated (assuming no carrier velocity saturation), the transconductance is modeled by the following expression:

$$g_m = \frac{\beta_e \beta_d (V_g - V_x - V_{td})(V_g - V_{te})}{(V_g - V_x)(\beta_e + \beta_d) - (\beta_e V_{te} + \beta_d V_{td})}$$

where V_g is the applied gate voltage, $V_x(\beta_e, V_g, V_{te}, \beta_d, V_{td})$ is the intermediate voltage between the two devices which is a function in and of itself, V_{td} is the threshold voltage of the depletion mode device, and V_{te} is the threshold voltage of the enhancement mode device.

β_e is the gain in the enhancement mode device and is given by

$$\beta_e = \frac{\mu_e C W}{L_e}$$

where μ_e is the mobility of the carriers in the enhancement mode channel, C is the gate capacitance per unit area, W is the width of the channel, and L_e is the length of the enhancement mode channel.

β_d is the gain in the depletion mode device and is given by

$$\beta_d = \frac{\mu_d C W}{L_d}$$

where μ_d is the mobility of the carriers in the depletion mode channel and L_d is the length of the depletion mode channel.

For the regime where both the depletion mode and enhancement mode devices are saturated, the transconductance is given by

$$g_m = \beta_e (V_g - V_{te})$$

with the variables defined as above.

compositional grading allows control of the surface material quality, strain fields due to misfit dislocations in the graded layer can lead to roughness at the surface of the epitaxial layer. If the roughness is severe, it will serve as a pinning site for dislocations and cause a dislocation pileup. An intermediate planarization step removes the surface roughness and thus reduces the dislocation density in the final epitaxial film. The smooth surface provided by planarization also assists in the lithography of the device and enables the production of fine-line features.

Subsequent processing of the heterostructures leads to alternative embodiments of the invention. Figures 12A and 12B are schematic block diagrams of alternative exemplary embodiments of LDMOS transistor structures in accordance with the invention. Figure 12A shows a structure 120 which includes a SiGe cap layer 122 provided directly on a bulk Si substrate 121 surface, with a strained Si epitaxial layer 123 provided on the cap layer. In the exemplary embodiment, the cap layer is, for example, a ~3-10μm thick uniform cap layer with ~30% content, and the strained Si layer ~25-300Å thick. Figure 12B shows a similar structure 124 including an insulating layer 125 embedded between the SiGe cap 122 and the bulk Si substrate 121. These substrates are produced by bonding a relaxed SiGe layer to a new Si (or SiO_2 coated Si) substrate, and then subsequently removing the original substrate and graded layer.

Figure 13 is a schematic block diagram of an exemplary embodiment of a buried channel LDMOS transistor device structure 130 in accordance with the invention. Figure 13 shows an initial heterostructure that has the conducting channel spatially separated from the surface via a cap region. In this exemplary embodiment, the charge carrier motion is distanced from the oxide interface, which induces carrier scattering, and thus the device speed is further improved. The structure 130 includes a Si substrate 131, a SiGe graded layer 132 (~1-4μm thick graded up to ~30% Ge content), a SiGe uniform layer 133 (~3-10μm thick with ~30% Ge content), a strained Si layer 134 (~25-300Å thick), a SiGe cap layer 135 (~25-200Å thick), and a second strained Si layer 136 (~25-200Å thick).

The second Si layer 136 is used to form the gate oxide of the device. When SiGe alloys are oxidized with conventional techniques, such as thermal oxidation, an excessive number of interfacial surface states are created, typically in excess of $10^{13}cm^{-2}$. In order to overcome this problem, a sacrificial Si oxidation layer is introduced into the heterostructure. The oxidation of this layer is carefully controlled to ensure that approximately 5-15Å of Si remains after oxidation. Since the oxide interface is in the Si and not the SiGe, the interfacial state density remains low, i.e., 10^{10}-$10^{11}cm^{-2}$, and device

CLAIMS

1. A heterostructure for a diffused metal oxide semiconductor (DMOS) transistor comprising:

a monocrystalline Si substrate;

a relaxed SiGe uniform composition layer on said substrate; and

a strained-Si channel layer on said uniform composition layer.

2. The heterostructure of claim 1, wherein a compositionally graded SiGe epitaxial layer is positioned between said Si substrate and said uniform composition layer.

3. The heterostructure of claim 1, wherein said strained-Si channel layer is spatially separated from the surface of the heterostructure.

4. The heterostructure of claim 3, wherein a semiconductor layer is provided on said strained-Si channel layer such that said strained-Si channel layer is buried below the surface of the heterostructure.

5. The heterostructure of claim 1, wherein an insulator is imbedded in between said strained-Si channel layer and said substrate.

6. The heterostructure of claim 1, wherein said relaxed SiGe layer is planarized prior to application of said strained-Si channel.

7. An integrated circuit comprising a heterostructure for a diffused metal oxide semiconductor (DMOS) transistor, said heterostructure comprising a monocrystalline Si substrate, a relaxed SiGe uniform composition layer on said substrate, and a strained-Si channel layer on said uniform composition layer.

8. The integrated circuit of claim 7, wherein a compositionally graded SiGe epitaxial layer is positioned between said Si substrate and said uniform composition layer.

9. The integrated circuit of claim 7, wherein said strained-Si channel layer is spatially separated from the surface of the heterostructure.

19. The integrated circuit of claim 17, wherein an insulator layer is imbedded in between said strained-Si channel layer and said substrate.

20. The integrated circuit of claim 17, wherein said relaxed SiGe layer is planarized prior to application of said strained-Si channel layer.

21. A method of fabricating a heterostructure for a diffused metal oxide semiconductor (DMOS) transistor comprising:

providing a monocrystalline Si substrate;

applying a relaxed SiGe uniform composition layer on said substrate; and

applying a strained-Si channel layer on said uniform composition layer.

22. A method of fabricating a heterostructure for a diffused metal oxide semiconductor (DMOS) transistor comprising:

providing a monocrystalline Si substrate;

applying a compositionally graded SiGe epitaxial layer on said substrate;

applying a uniform composition SiGe cap layer on said graded layer; and

applying a strained-Si channel layer on said cap layer.

23. A method of fabricating a heterostructure for a diffused metal oxide semiconductor (DMOS) transistor comprising:

providing a monocrystalline Si substrate;

applying a relaxed SiGe uniform composition layer on said substrate;

applying a first strained-Si channel layer on said uniform composition layer;

applying a SiGe cap layer on said strained-Si channel layer; and

applying a second strained-Si layer on said cap layer.

24. A method of fabricating a heterostructure for a diffused metal oxide semiconductor (DMOS) transistor comprising:

providing a monocrystalline Si substrate;

applying a compositionally graded SiGe epitaxial layer on said substrate;

applying a uniform composition SiGe layer on said graded layer;

applying a first strained-Si channel layer on said uniform composition SiGe layer;

applying a SiGe cap layer on said strained-Si channel layer; and

applying a second strained-Si layer on said cap layer.

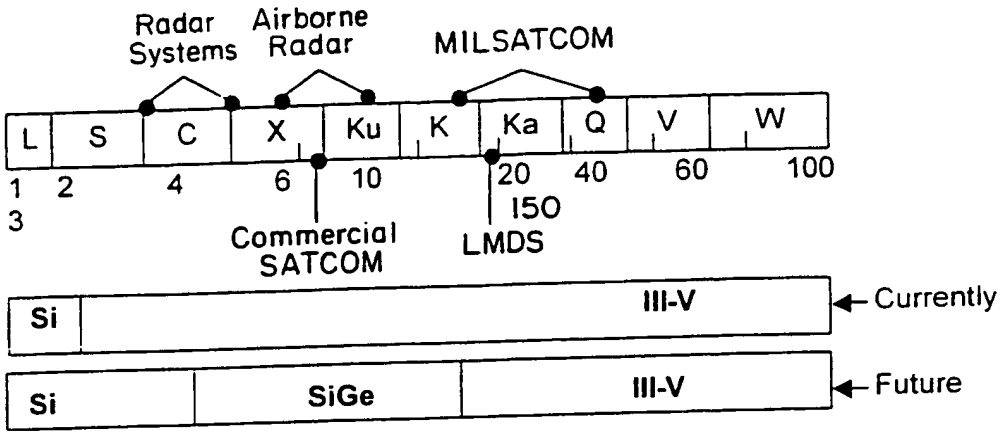


FIG. 3

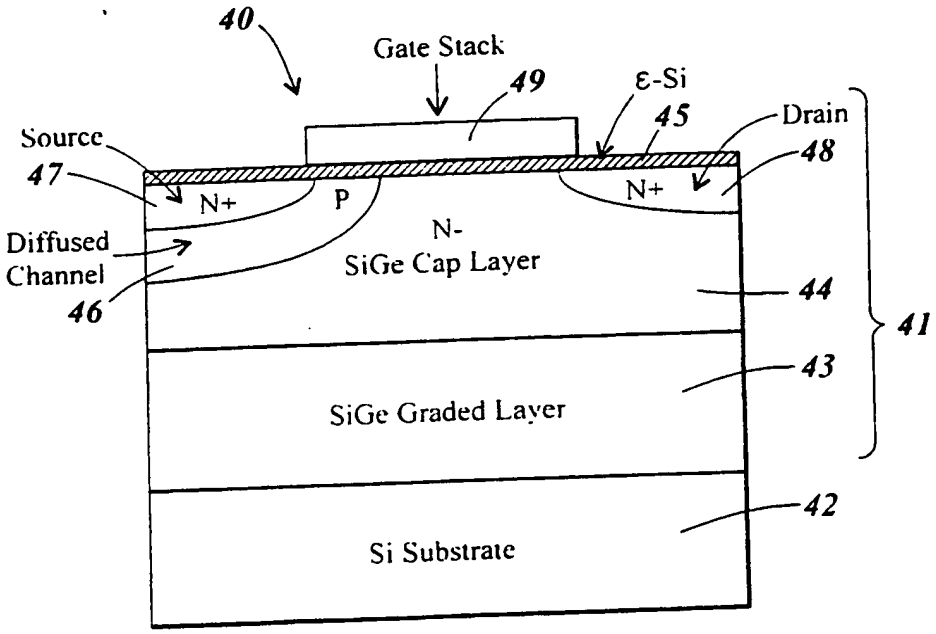


FIG. 4

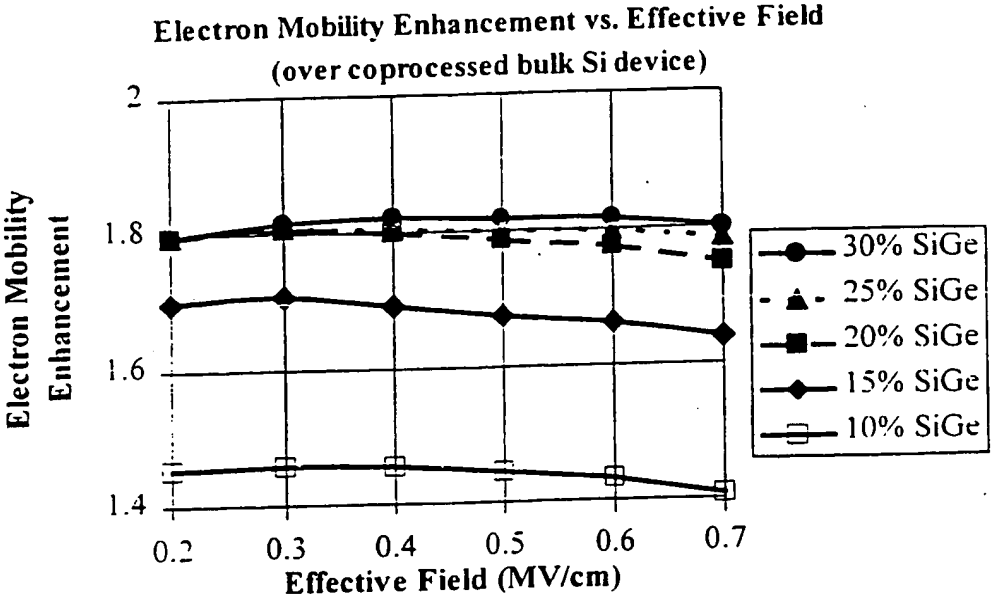


FIG. 7A

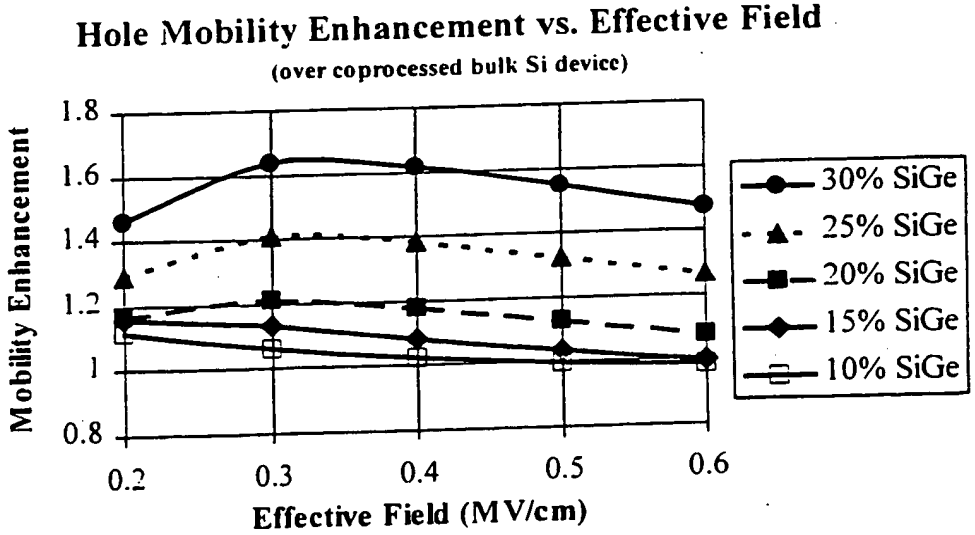


FIG. 7B

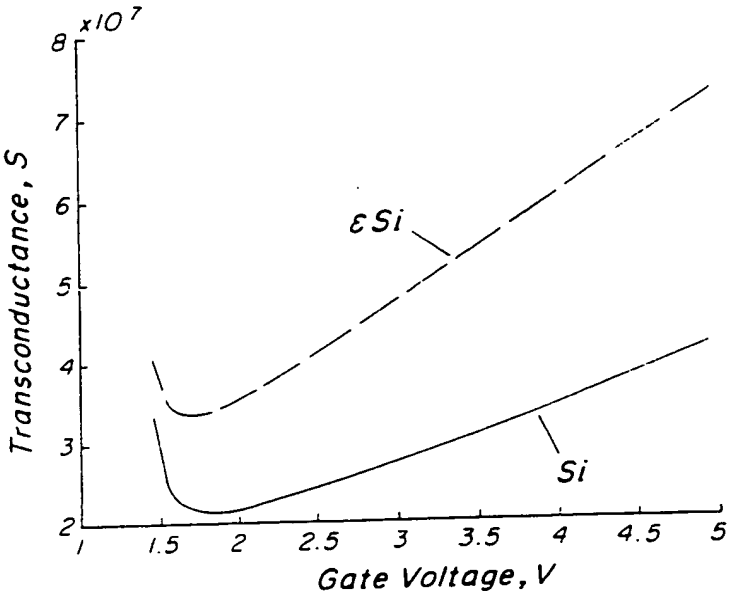


FIG. 10

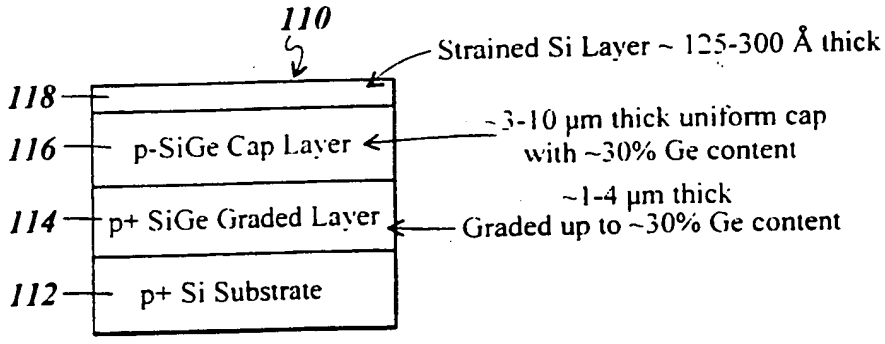


FIG. 11

INTERNATIONAL SEARCH REPORT

Int. .tional Application No
PCT/US 01/01730

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/10 H01L21/336 H01L29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 906 951 A (CHU JACK OON ET AL) 25 May 1999 (1999-05-25) column 2, line 40 -column 4, line 5; figures 1-5 ---	1-24
X	US 5 759 898 A (PITNER PHILIP MICHAEL ET AL) 2 June 1998 (1998-06-02) column 2, line 66 -column 4, line 6; figures 1,2 --- -/--	1,5-7, 11,12,21

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int .tional Application No
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